**Chapter 5: BUSES IN 8085**

**Topic – 1: Requirement Of Buses**

**Introduction**

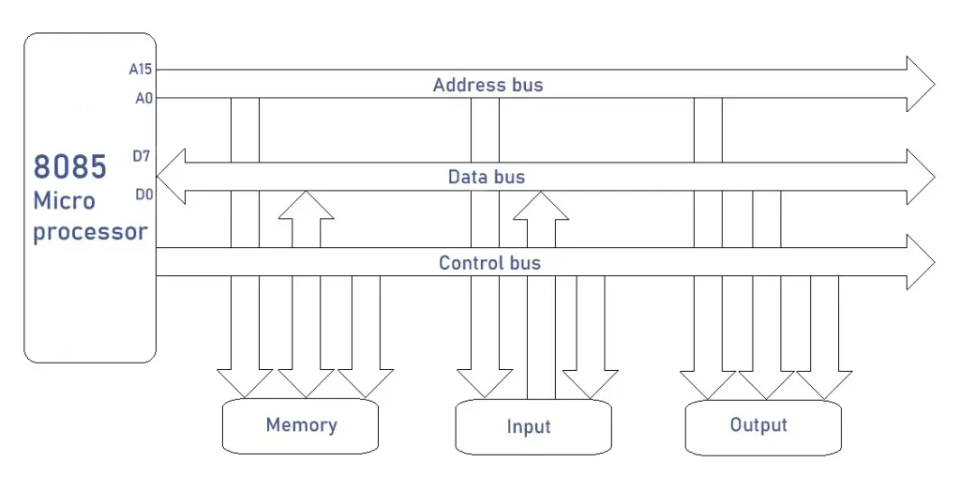
* Provides **connection** between many devices across microprocessor.
* It is because of buses only that **CPU**, **memory** & **peripherals** can communicate.

**Types Of Buses**

* **Serial buses:** Data are transferred **bit by bit** in a **single line**.
* **Parallel buses:** Bits of data are transferred **parallelly** through **multiple lines**.
* **8085** has parallel type of bus.

**Topic – 2: Bus Structure**

**Diagram**



***\*The arrows show if a bus is unidirectional or bidirectional\****

**Types Of Buses In 8085**

* **Address bus:** Even address of **I/O** device is transferred through it.
* **Data bus:** **8-bit** wide, as 8085 is an **8-bit** microprocessor.
* **Control bus:** Used to **transfer signals** across the microprocessor.

**Topic – 3: Types Of Buses (Descriptive)**

**Address Bus**

* Carries **address** of data to be read or written.
* **16-bit** bus with **parallel** lines.
* **Hex** addresses are converted to **binary** & then **transferred**.
* Supports **216 bytes = 64 kilo bytes**

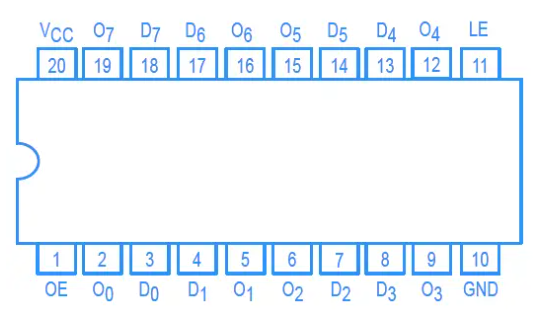
**Data Bus**

* **8-bit** long on width.
* **Bidirectional**, as data flow in both directions to **read** & **write**.
* For **output** processes, **write** operations are performed & for **input**…
* Each bit requires a pin but 8085 keeps it low using **multiplexers**.
* **AD0 – AD7** serve **dual** purpose, with functionalities of both **address** & **data bus**.
* To access **lower** **8-bits** of an address, we need to demultiplex **AD0 – AD7**.

**Topic – 4: Lower Bit Addresses**

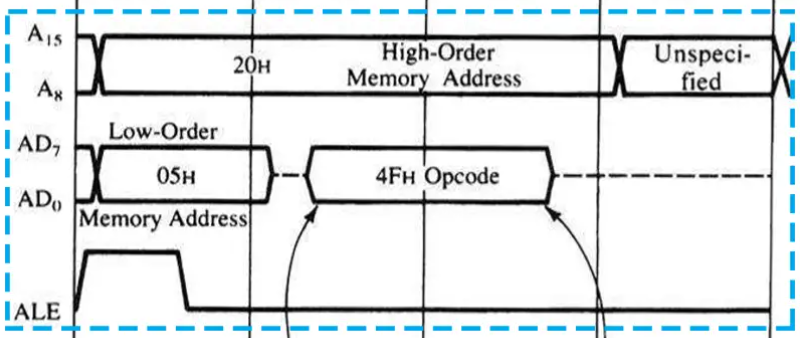
**Demultiplexing of AD0 – AD7 Using IC 74LS373**

* We can make pins **multifunctional** but it requires additional complex circuit to be made.



* **IC 74LS373** has **eight latches**, each controlled by **two signals**.
* These signals are **LE** (latch enable) & **OE** (output enable).
* So, there are **eight pairs** of **input** and **output** pins.
* When **LE** is **high**, the input at **D0 – D7** are reflected at **O0 – O7**.
* And the **OE** is high all the time.

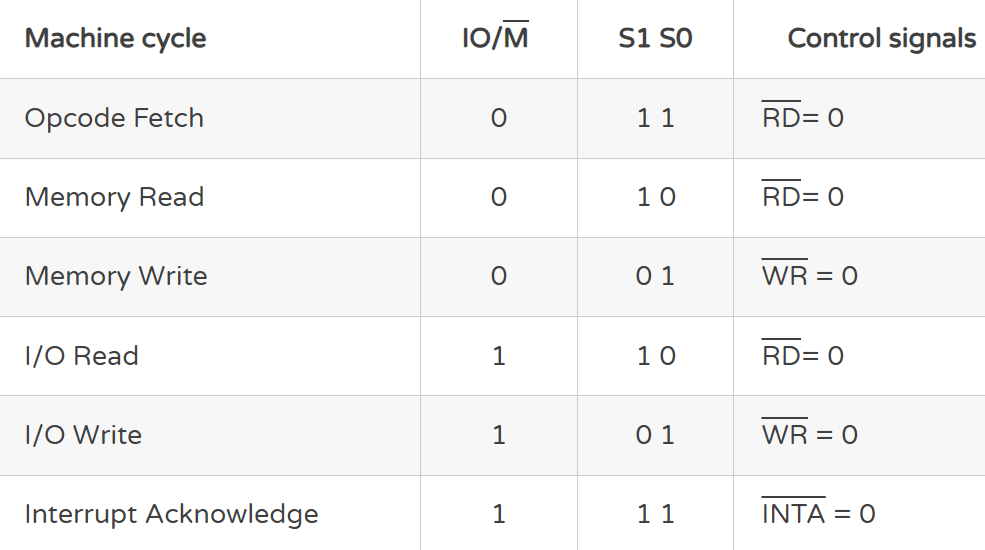
**Timing diagram of AD0 – AD7**



* At this time the **ALE pin** is high means that pins are currently working as **address pins**.
* When an instruction is executed, both its **opcode** & **addresses** need to be fetched.
* So, after the **address** is fetched, it is stored in **latches** & then the pins work as **memory pins**.
* **AD0 – AD7** pins fetch the **lower bits** & **A8 – A15** pins fetch the **higher bits**.
* Then after this, the data is fetched in **2nd** & **3rd** clock cycle.
* At this time, the pins are being used as **data bus**.

**Topic – 5: Control Bus**

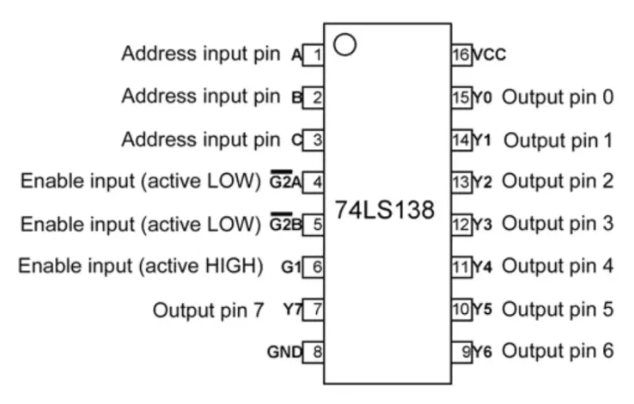
* Pins used in this bus are **IO/M**, **WR**, **RD**.
* These pins use **control signals** to make their operations.
* **IO/M** tells if the **WR/RD** operation is being performed on **input** or **output** device.



**Topic – 6: 74LS138 Decoder IC**

**Introduction**

* **74LS138** is a **3:8** decoder.
* Interfacing **IO/M** pin with **WR** and **RD** pins make things a little complex.



* Input pins – **A**, **B** & **C**.
* Output pins – **Y0 – Y7**
* The **active low input** **pins** are connected to **GND** & **active high input** **pin** is to **VCC**.

**Interfacing 74LS138 With 8085**

